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Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout

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A prototype hadronic calorimeter for the ILC detector is under construction at DESY. It will consist of 8000 scintillator tiles with analog readout performed via SiPM directly mounted on each tile. A dedicated ASIC chip has been developed to match the requirements of large dynamic range, low noise, high precision and large number of readout channels needed.
Particular care is given to the optimization aspects of the ASIC chip in the SiPM readout chain. To fully exploit the self-calibrating potentiality of this photo-detector device, capable of recording single photo-electron signals, an externally selectable gain and shaping time are included in the design.
The calorimeter system is described and the first calibration data are presented.

1 An hadronic calorimeter for the ILC

The requirements imposed by the high precision physics at the International Linear Collider (ILC) set high demands on calorimetry. For excellent separation of WW jets from ZZ jets, which plays a key role in Higgs boson studies, a jet-energy resolution of $\sigma_E/E \sim 0.3/\sqrt{E}$ is required [1]. This can be achieved by combining the potentials of the particle flow approach with high granularity in transverse and longitudinal directions for both electromagnetic (ECAL) and hadronic (HCAL) calorimeters.
The ECAL design is based on a Si/W sampling structure with sensitive silicon pads of 1 cm^2 surface. The prototype will consist of approximately 10,000 channels. The prototype and readout electronics have been developed by LAL [2].
A sub-group of the CALICE collaboration [a] has developed the analog option for the HCAL based on a sampling structure with scintillating tiles (of smallest

[a] The institute members of the group are: DESY, Hamburg U, ICL (London), ITEP (Moscow), LAL (Orsay), LPI (Moscow), MEPHI (Moscow), Northern Illinois U., RAL, UCL (London).

size $3\times3\times0.5$ mm^3) individually readout by Silicon Photo-Multiplier (SiPM) mounted on each tile.

The SiPM is a pixelated avalanche photo-diode operated in limited Geiger mode. The detector surface of 1×1 mm^2 is divided into 1156 pixels. The analog output is obtained by adding the response of all pixels fired as independent digital counters. The SiPM are operated at 2-3 volts above breakdown voltage. Given that the internal pixel capacitance C_{pixel} is typically 50 fF the charge collected for one photo-electron signal is $\sim$160 fC (or $\sim10^6$ electrons). The SiPM offer a very fast response with a typical rise time of the order of a nanosecond. The fall time of the signal depends on the pixel quenching resistor and can be tuned to the needs of the experimental application (typical values are between 20-500 ns). The dynamic range is determined by the finite number of pixels and is $\sim$200 pC.
In order to test the feasibility of the particle flow approach prototypes of both ECAL and HCAL are being built by the CALICE collaboration and will be tested in a combined test beam experiment.

To meet the needs of the analog HCAL prototype it was decided to adapt the chip designed for the ECAL front-end electronics [6] to read the SiPM signal. In the following the main features of this ASIC chip are described and its properties analyzed.

2 Very front-end electronics description and properties

The main tasks of the very front-end electronics are to fine tune the bias voltage applied to each SiPM; to decouple, from the same line, the charge signal and to preamplify it such that it can be transported to the front-end electronics a few meters away from the detector.
The very front-end electronics should also give the possibility to reduce the number of readout lines to be transported to the front-end electronics. Furthermore, the readout system has to match the DAQ requirements and the trigger constraints at the test beam. A delay of approximately 150 ns is estimated between the beam crossing the trigger counters system and the time at which the trigger signal is formed and received at the very front-end.
All this tasks are fulfilled by the ASIC chip (ILC-SIPM) and the very front-end electronics designed to steer it.

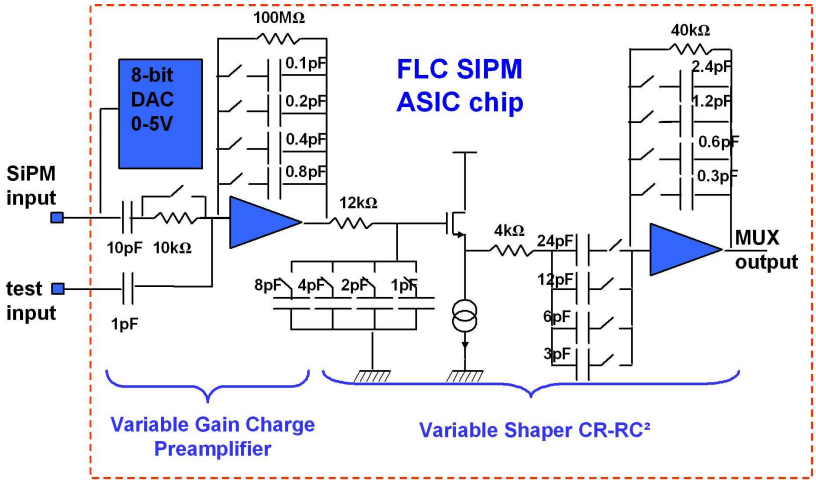

Figure 1: Schematic view of ASIC chip components.

2.1 ASIC Chip description

An 18-channel ASIC chip dedicated to SiPM readout has been developed starting from the design, in AMS 0.8 μm CMOS technology, already in use for the Si-W ECAL prototype readout. Fig. 1 shows a schematic view of this ILC-SIPM ASIC chip. The integrated components allow the choice between 16 selectable preamplification gain factors from 1 to 100 mV/pC, and between 16 CR(RC)^2 shapers with shaping times from 40 to 180 ns. A 10 kΩ resistor can be add at the input of the preamplifier to further delay the signal peaking time (at the expenses of a 40% noise increase).
After shaping the signal is held at its maximum amplitude with a track and hold method and multiplexed by an 18-channel multiplexer to provide a single analog output to the ADC. An example of the signal path through the chip is given in Fig. 2a-d, where the stages of input, amplified and shaped, held and multiplexed signal are shown. The longest shaping time has been introduced in the ECAL design to match the long delay of the beam trigger in a test beam environment ($\sim$150 ns). For SiPM gain calibration using LED signal, pile-up from thermal noise-induced signals (dark rate) can be reduced by exploiting the fast SiPM response with a shorter shaping time.
The large variety of operation modes offered by the ASIC chip gives the opportunity to amplify more that only the SiPM signals with the same chip design. This is a big advantage as signals from monitoring devices like PIN-diodes or

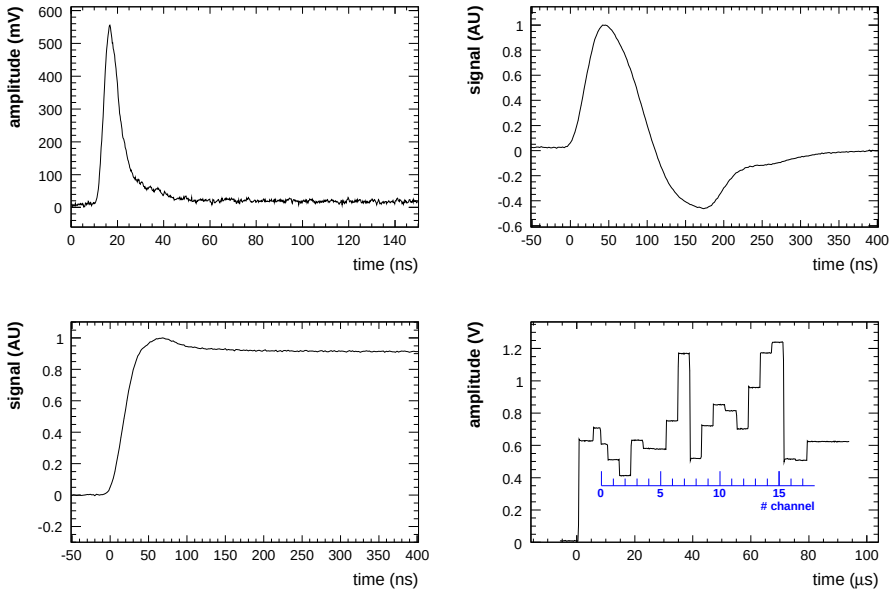

Figure 2: Electrical signal processing in the ASIC.a) Input (x18), b) preamplified and shaped (x18), c) held (x18), d) multiplexed (x1) signal.

photo-multipliers can be read out over the same chain.

A 5V rail-to-rail 8-bit Digital to Analog Converter (DAC), integrated on each of the 18 input lines of the ASIC chip, allows individual adjustment of the SiPM bias voltage for each channel. In addition to the 18 signal inputs the ASIC chip provides two test inputs (each one common to 9 channels) to check the preamplification line decoupled from the SiPM.

The properties of the ASIC chip relevant to the operation in conjunction with the SiPM have been tested using the test setup sketched in Fig. 3.

2.2 Linearity

The study of the linearity range of the ASIC chip for various combinations of gain and shaping time has been performed injecting current from an external capacitor (C1) to the ASIC chip input. By varying the value of the capacitor C1 it is possible to change the duration of the injected charge to mimic the

real shape of a SiPM signal. Fig. 4 demonstrates how the shape of the input

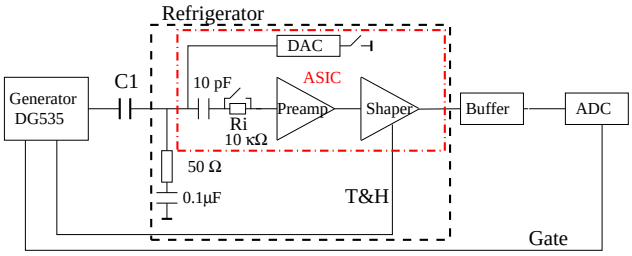

Figure 3: Electronic set up for ASIC chip studies.

signal is adjusted choosing a 68 pF capacitor.
Each input channel of the ASIC chip is grounded via a 50 Ohm resistor and a 0.1 μF capacitor.
The output signal of each preamplifier and shaper stage is held at its maximum value by an external track & hold signal timed with the generator. The duration of the hold time is determined by the width of the hold signal, generally about 2-5 μs. A signal amplitude drop of 1 mV per 500 ns is observed. During this time the signal is measured on a peak sensing 11-bit ADC with a gate of 100-400 ns.
The linearity range of the ASIC chip operated with longest shaping time (∼180

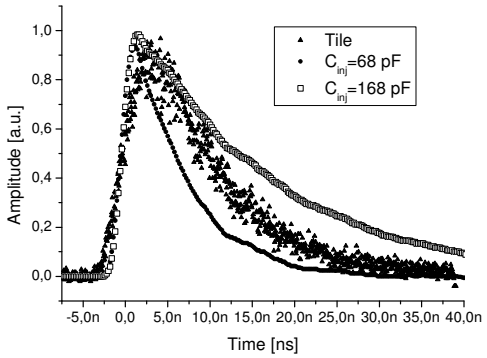

Figure 4: Comparison of charge injected signal to real SiPM signal.

ns) is presented in Fig. 5a. The saturation of the input charge is visible which

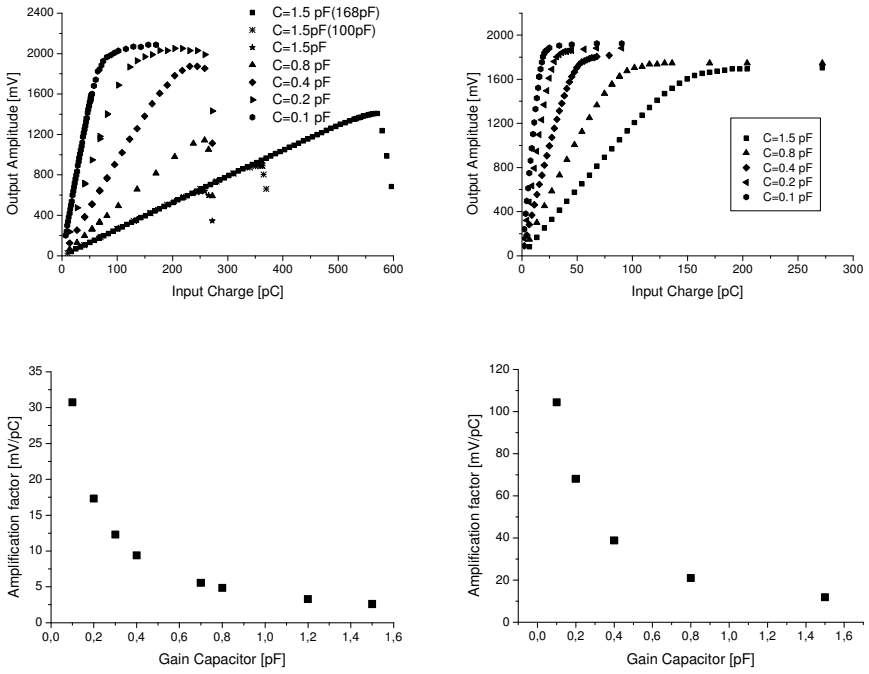

Figure 5: Linearity of ASIC chip output signal for the longest (a) and shortest (c) shaping time and various gains. b-d) Relative gain factors as a function of the chosen capacitor.

depends on the shape of the injected signal (or the value of the input capacitor C1). In Fig. 5b the gain factors for the various choices of capacitors are shown, which are calculated from a fit to the linear (± 3 %) part of the curves in Fig. 5a.

The same values are evaluated from Fig. 5c and shown in Fig. 5d for the shortest shaping time (∼40 ns). It can be observed that for low capacitors the increase of the gain value is not linear with the increase of the capacitor value. If the input is not saturated, the ASIC chip output saturates between 1.7 and 1.9 V depending on the gain. While the slopes of the curves in Fig. 5a(c), as well as the absolute gain values reported in Fig. 5b(d), are strongly changing depending on the value of the input capacitor C1, the output saturation level stays quite constant. We conclude that the ASIC chip can be used for SiPM-

like signal readout in a linear range up to 1.3 V for all combinations of gains and shaping times.

2.3 Noise

In order to measure the noise contribution of the ASIC chip preamplifier the input line was grounded only via the 50 Ohm resistor in Fig. 3, removing the 0.1 μF capacitor. In this way, the noise of the DAC component is neglected. The noise is defined as the standard deviation (σ) of the Gaussian fit to the

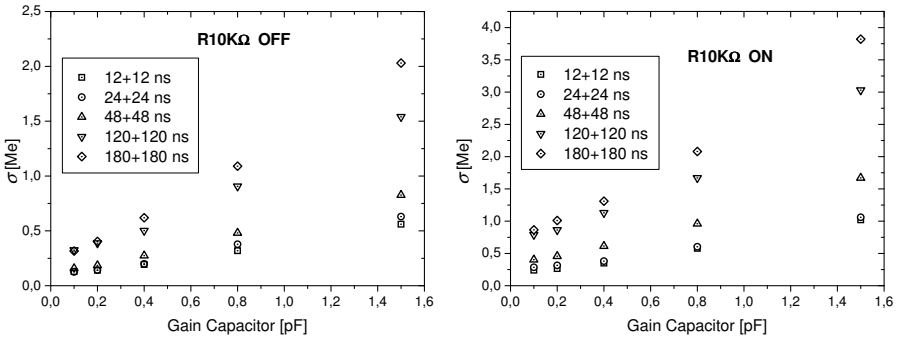

Figure 6: Noise of the ASIC chip preamplifier, expressed in units of 10^6 electrons (Me), for various combinations of gains and shaping times. Bypassing (left) or using (right) the 10 kΩ injection resistor Ri.

noise spectrum of the ASIC chip for various combinations of gains and shaping times. In Fig. 6 the noise values are presented for the two operation modes in which the injection resistor (Ri) is used or bypassed. The noise is expressed in units of 10^6 electrons (Mega-electrons = Me).
The amplitude of the SiPM signal for a single pixel firing (one photon signal) is approximately 1 Me, therefore the electronic noise should be smaller than this value to resolve single pixel structure. The best noise to gain ratio of 0.25 Me is obtained for the highest gain and the shortest shaping time, which is the mode adopted for single pixel calibration in the operation with SiPM.

2.4 Individual channel voltage adjustment (DAC)

As previously discussed, one of the requirements of the developed very front-end electronics is to operate a large number of SiPM, being able to individually

steer their bias voltage. This is achieved by a voltage adjustment via a 8-bits DAC connected to the input of each ASIC chip preamplifier channel. The DAC covers effectively the range between 0.24 and 4.7 V, in steps of 20 mV. In Fig. 7 the linear range of the DAC output voltage is shown together with its noise. The voltage stability required for SiPM operation is on the order of 30 mV, corresponding to a change in gain for the SiPM of about 1%. The

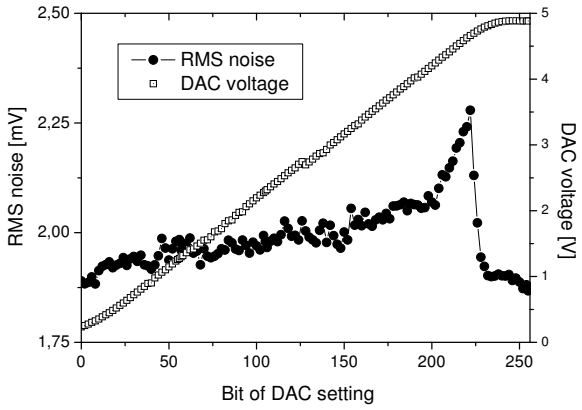

Figure 7: DAC output voltage and noise as a function of DAC setting parameter.

stability of the DAC is very well below this level.
A check was made to ensure the input of the DAC could tolerate the typical current from the coupling to the SiPM (5-0.3 μA). The maximum tolerable current at the DAC input was found to be 40-140μA depending on the DAC settings, compatible with the requirements. From this the dissipation power of the DAC has been calculated to be about 500 μW.

2.5 Temperature dependence of the ASIC

The SiPM response is dependent on temperature and bias voltage variations, in particular the temperature variation of the SiPM gain at room temperature is measured to be 4.5%/°K.
The temperature dependence of the ASIC chip has also been investigated to ensure its minor contribution to the system. For this purpose one ASIC chip with its driving board have been placed into a thermal box where the temperature what varied between 10 and 70°C.

The temperature dependence of the ASIC chip signal has been measured for two combinations of gain and shaping time (G=0.5 pF and T=180 ns referred to as physics mode, G=0.1 pF and T=40 ns referred to as calibration mode) and for both the signal and the test input channels of the ASIC chip.
In all cases it is found that the time peak position and the signal noise do not depend of temperature. The temperature dependency of the gain is summarized in table 1 for all investigated combinations.

ASIC chip input	signal	test input
$\Delta G/\Delta T$ (calibration mode)	-0.27%/°K	-0.12%/°K
$\Delta G/\Delta T$ (physics mode)	-0.11%/°K	-0.021%/°K

Table 1: Temperature dependence of ASIC chip gain.

3 SiPM readout with the ASIC chip

Once established that all the ASIC chip characteristics are compatible with the type of signal and the requirements for which the chip was designed, one can proceed and integrate the SiPM to its very front-end electronics and study the property of the combined system.
The studies presented in this section are performed for one single channel, to understand the effect of the readout electronics on the SiPM signal. The operation of a large number of SiPM with the same very front-end electronics will be discussed in a dedicated publication.
The connection scheme of SiPM to the ASIC chip is shown in Fig. 8. The possibility to calibrate the SiPM gain is an important advantage of this type of photo-detector. For this it is necessary to measure the separation of the

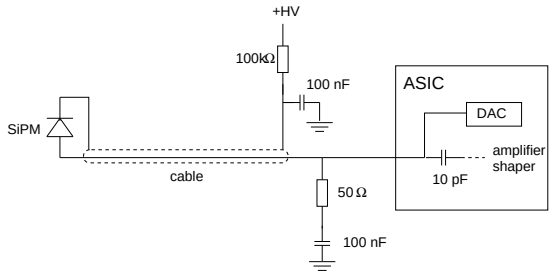

Figure 8: Connection scheme of SiPM to ASIC chip.

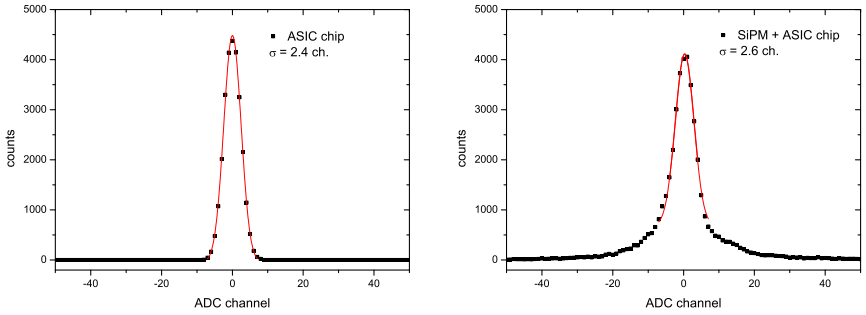

Figure 9: Noise spectrum from the ASIC chip only (a) and SiPM connected to the ASIC chip (b). In both plots the fit interval is fixed to be $\pm 3\sigma_{el}$, with $\sigma_{el} = 2.4$ ADC channels.

single pixel peaks in the SiPM pulse hight spectrum. To achieve best separation with minimum noise contribution from the electronics and from the SiPM dark rate, the mode adopted to perform gain calibration is the combination of the highest gain (G=0.1 pF) and the shortest shaping time (T=40 ns).
The analog SiPM signal (not held) at the ASIC chip output is shown in Fig. 2b. The bipolar shape of the signal is obtained after the CR(RC)^2 shaper. Due to the SiPM dark rate the noise spectrum obtained with SiPM connected to the ASIC chip (Fig. 9b) deviates from the perfect Gaussian shape resulting only from electronic noise (Fig. 9a). The positive and negative tails in Fig. 9b are the result of thermal noise-induced signals hold at their positive or negative amplitudes. Due to the different amplification of the positive and negative parts of the bipolar signal the spectrum in Fig. 9b is asymmetric. To estimate the width of the zero peak in this case the Gaussian fit-function is limited to $\pm 3\sigma_{el}$, where σ_{el} is taken from the fit to the electronic noise only (Fig. 9a). The values obtained are $\sigma_{el} = 2.4$ ADC channels and $\sigma_{el+SiPM} = 2.6$ ADC channels, corresponding to $\sim$0.2 photo-electrons. The purpose of this comparison is to demonstrate that the ASIC chip is suited to readout SiPM signal and the combined noise does not increase significantly when connected to SiPM. On the other hand, this measurement shows that the combined noise is dominated by the electronic noise, a point that can be improved in the next generation of ASIC chip for SiPM readout.

Using a low intensity light source it is possible to observe the single pixel structure in the SiPM pulse hight spectrum, as seen in Fig: 10. The separation of subsequent peaks is good and allows for a multi-Gaussian fit to determine the

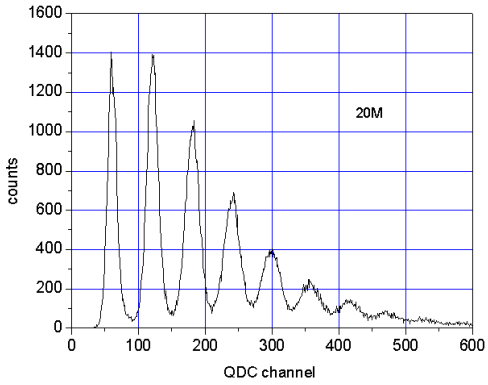

Figure 10: Single photo-electron peak spectrum from SiPM with ASIC chip readout.

SiPM gain $\Delta peaks$ (here shown in QDC channels and not recalibrated to Me) and the peak widths. The signal to noise ratio obtained for single pixel signal is ∼4, in agreement with the ratio extracted from the direct measurements of the ASIC chip in section 2.3.
During normal data taking the SiPM signal amplitude can vary up to the SiPM saturation which, for the 1156-pixel device used for the HCAL prototype, is at about 1250 effective pixels fired or 200 pC. It is possible to choose the preamplifier gain such that the amplified signal is contained in the linear range of the ASIC chip. The shaping time chosen for beam or cosmics data taking is fixed to the longest possible (T=180 ns) by the requirement of the external trigger latency. It has been checked that choosing an intermediate gain (G=0.5 pF) the SiPM signal saturates below the limit value of 1.3 V fixed to be in the ASIC linear range at the 3% level. For this choice of gain the combined noise of ASIC chip and SiPM allows a signal to noise separation for minimum ionizing signal of ∼5, sufficient for the planned application in a hadronic calorimeter prototype.

4 Conclusions

After this series of measurements we conclude that the ASIC chip ILC-SIPM developed by LAL, together with the very front-end electronics designed to steer it, can be used to readout and calibrate SiPM photo-detectors.

The dedicated very front-end electronics provides the possibility to control the bias voltage applied to the SiPM with a low noise DAC. It allows to perform SiPM gain calibration with a signal to noise ratio for single photon signal of $\sim$4. Furthermore, it offers the required linear dynamic range to readout the signal from a 1156-pixel SiPM, of the type used in the hadronic calorimeter prototype for the ILC.

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